AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Canceled)

2. (Canceled)

3. (Currently amended) ~~The verification test bench system~~ A system for verifying a core of a system on a chip (SOC) of claim ~~2~~ 21, wherein said bi-directional general purpose I/O device is coupled between said ~~design~~ core of a system on a chip (SOC) and said bus functional model, and transfers said directives between said design and said bus functional model.

4. (Currently amended) The ~~verification test bench system~~ system for verifying a core of claim ~~2~~ 21, wherein ~~said~~ control code in said bus functional model responds to said directives by configuring said mirror interface for said exchange of data.

5. (Currently amended) The ~~verification test bench system~~ system for verifying a core of claim 4, wherein said control code verifies results of said exchange of data.

6. (Canceled)

7. (Currently amended) The ~~verification~~ system for verifying of claim ~~6~~ 21, said control mechanism comprising:

a standardized handshake protocol for communicating with said SOC; and

control code for configuring said mirror interface and transferring data to said external interface via said mirror interface.

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Canceled)

13. (Currently amended) The method of claim ~~12~~ 22, wherein said control mechanism comprises:

a standardized handshake protocol for communicating with said SOC; and

control code for configuring said mirror interface and transferring data to said external interface via said mirror interface.

14. (Original) The method of claim 13, further comprising issuing directives in said handshake protocol to said control code, to configure said mirror interface and initiate data transfer between said mirror interface and said external interface.

15. (Currently amended) The method of claim ~~11~~ 22, ~~further comprising connecting~~ a wherein said bus functional model ~~to said mirror interface, to provide~~ provides processor bus cycles for driving said mirror interface.

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Previously presented) A system for verifying an external interface of a core of a system on a chip (SOC) comprising:

a mirror interface having the identical input and output connections of said external interface;

a bus functional interface connected to said mirror interface for modeling an internal bus, said bus functional interface having a processor model for emitting CPU cycles which emulate a processor, a control mechanism which controls the flow of data through the external interface and to apply test stimuli from the mirror interface to the external interface, and a memory to receive any data transferred from the external interface; and

an external bi-directional general purpose I/O connected to said SOC to transfer control directives to configure the mirror interface through the bus functional interface for a given test case being executed in said SOC, and to exchange data between the external interface and mirror interface during the given test case.

22. (New) A method for verifying an external interface of a core of a system on a chip (SOC) comprising:

modeling a mirror interface which is a copy of said external interface with a bus functional model so that said mirror interface and external interface can exchange data, and said bus functional model can control the flow of data through said external interface;

generating directives from a test case executing in said SOC to configure said mirror interface and transferring to the bus functional model said directives through an external bi-directional general purpose I/O control;

applying a test stimuli from the mirror interface to the external interface;

exchanging data between the external interface and mirror interface during a given test case; and

storing in memory said data transferred from said external interface through said mirror interface.

23. (New) A computer program product for storing instructions for verifying an external interface of a core of a system on a chip (SOC), said instructions carrying out the steps of:

modeling a mirror interface which is a copy of said external interface with a bus functional model so that said mirror interface and external interface can exchange data, and said bus functional model can control the flow of data through said external interface;

generating directives from a test case executing in said SOC to configure said mirror interface and transferring to the bus functional model said directives through an external bi-directional general purpose I/O control;

applying a test stimuli from the mirror interface to the external interface;

exchanging data between the external interface and mirror interface during a given test case; and

storing in memory said data transferred from said external interface through said mirror interface.